REMARKS/ARGUMENTS

Reconsideration of the application is requested.

Claims 1-13 and 27-39 remain in the application. Claims 1-13 and 27-32 are subject to examination and claims 33-39 have been withdrawn from examination. Claims 1 and 27 have been amended. Claims 15-26 have been canceled herewith.

Under "Claim Objections" on page 2 of the above-identified Office Action, the Examiner stated that if claims 2-13 were found allowable he would object to claims 15-26 (under 37 CFR 1.75 and MPEP § 706.03(k)) because claims 15-26 are a substantial duplicate of claims 2-13.

Claims 15-26 have been canceled herewith and therefore, obviate the Examiner's potential objection to these claims.

In the second paragraph under item 3 on page 2 of the above-identified Office Action, claims 1, 2-6, 8-10, 12, 13, 15-19, 21-23, 25, and 26 have been rejected as being obvious over/fully anticipated by Hofmann et al. (U.S. Patent 6,191,459) (hereinafter "Hofmann") under 35 U.S.C. § 102(a).

The rejection has been noted and claims 1 and 27 have been amended to even more clearly define the invention of the instant application. Support for the changes is found in the previous claims and the drawings of the instant application.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful. Claim 1 calls for, *inter alia*, a memory cell having:

a semiconductor component having semiconductor material having an upper surface;

the semiconductor material having a trench formed therein and a gate electrode located in the trench; and

a memory transistor including **a source region and a drain region formed at the upper surface of the semiconductor material**, the memory transistor including **the gate electrode** located on the top side and **located in a lateral direction between the source region and the drain region, the source region and the drain region being located on opposite sides of the trench**. (emphasis added)

Claim 27 calls for, *inter alia*, a memory cell configuration, having:

a semiconductor material having an upper surface;

a plurality of memory cells that each include:

> a memory transistor including **a source region and a drain region formed at the upper surface of the semiconductor material**, the memory transistor including a **gate electrode located in a lateral direction between the source region and the drain region, the source region and the drain region being located on opposite sides of each one of the plurality of trenches**;

the gate electrode of each one of the plurality of memory cells being located in a respective one of the plurality of trenches. (emphasis added)

Hofmann does not disclose a structure having a gate electrode configured and laterally disposed between source and drain regions located on opposite sides of a trench that are formed at the same upper surface of semiconductor material as recited in the claims. Hofmann discloses a memory cell array

having source and drain regions that are alternatively situated at the upper surface of the semiconductor body and at the bottom of trenches formed therein. The present invention uses the trench bottoms as channel regions.

The Examiner has taken the position that in Hofmann the device surface is the total semiconductor surface including sidewalls and bottoms of the trenches. Independent claims 1 and 27 have been amended to clearly patentably distinguish the present claimed invention over Hofmann by reciting that the source and drain regions are in the **upper** surface and the **lateral** orientation of the gate with respect to the source and drain on opposite sides of the trench. Such an arrangement is not shown in Hofmann where the source 10a is at the bottom of a trench and the drain 10b is at or near the top of the trench and the gate 18 is vertically disposed above the source and laterally disposed relative to the drain. This arrangement is not the same as the source/drain regions being arranged at the upper surfaces of the device between the trenches, while sidewalls and bottom of the trenches beneath the source/drain regions form the transistor channel. The gate electrodes are arranged in between the source and drain regions on opposite sides of each trench.

Hofmann does not show "a source region and a drain region formed at said upper surface of said semiconductor material, said memory transistor including said gate electrode located on said top side and located in a lateral direction between said source region and said drain region, said source region and said drain region being located on opposite sides of said trench" as recited in claim 1 of the instant application. claim 27 contains similar limitations.

In paragraph A under item 4 on page 5 of the above-identified Office Action, claims 27, 28, and 29 have been rejected as being unpatentable over Bate (U.S. Patent 4,360,900) in view of Hofmann under 35 U.S.C. § 103(a).

Bate does not disclose an arrangement of the source/drain regions at the upper surfaces of the device between the trenches and an arrangement of the gate electrodes in between the source and drain regions on opposite sides of each trench. Bate discloses an arrangement of the gate electrode above the semiconductor body comprising the source and drain regions as doped regions. Claims 1 and 27 now define the lateral orientation of the gate with respect to the trench and the drain/source regions, in a manner that is not disclosed or suggested by Bate (or Hofmann).

Bate does not disclose the claimed memory cell structure. In Bate the titanium dioxide layer 25, 45 is an intermediate layer between the aluminum layer 26 provided as the gate electrode and the memory layer structure used to store charge carriers and comprising an Si_3N_4 layer 23, 43 as a storage layer. The purpose of this intermediate layer and of the chosen materials is to shift the main voltage drop into the storage layers. The storage layers comprise standard sequences of silicon oxide and silicon nitride.

Bate does not disclose a structure having a gate electrode configured laterally between source and drain regions on opposite side of the trench. Bate discloses planar devices as shown in Figs. 3a and 7a. The source and drain regions are formed in the substrate, whereas the gate electrode is formed by a layer located above the source and drain regions.

Bate does not disclose "said semiconductor material having a plurality of trenches formed therein; a plurality of memory cells that each include: a memory transistor including a source region and a drain region formed at said upper surface of said semiconductor material, said memory transistor including a gate electrode located on said top side and located in a lateral direction between said source region and

said drain region, said source region and said drain region being located on opposite sides of each one of said plurality of trenches" as recited in claim 27 of the instant application.

The foregoing discussion of Hofmann applies equally to this rejection. It is apparent that Hofmann not only has its own deficiencies as a reference relative to the instant claims, but also does not make up for the deficiencies of Bate.

In paragraph B under item 4 on page 7 of the above-identified Office Action, claims 7, 11, 20, and 24 have been rejected as being unpatentable over Hofmann in view of Bate under 35 U.S.C. § 103(a).

The foregoing discussions of Hofmann and Bate are equally applicable in the rejection of claims 7, 11, 20, and 24, which depend from and incorporate the limitations of independent claim 1.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of independent claim 1 or 27. Claims 1 and 27 are, therefore, believed to be patentable over

the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claim 1 or claim 27.

Applicants appreciatively acknowledge the Examiner's statement that claims 30-32 "would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims." In light of the above, applicants respectfully believe that rewriting of claims 30-32 is unnecessary at this time.

In view of the foregoing, reconsideration and allowance of claims 1-13 and 27-32 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out. In the alternative, the entry of the amendment is requested, as it is believed to place the application in better condition for appeal, without requiring extension of the field of search.

If an extension of time for this paper is required, petition for extension is herewith made.

Please charge any other fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

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For Applicant(s)

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